IN THE SPECIFICATION

Please amend the Specification as follows:

(1) Please replace the paragraph beginning at line 16, page 6 with the following rewritten paragraph:

~~Figure 7~~ Figures 7A-D illustrate[[s]] a spreadsheet used to identify pin locations on a chip in a multiple chip module that should be used for diagonal or orthogonal signal pins.

(2) Please replace the paragraph beginning at line 24, page 14 and ending at line 18, page 15 with the following rewritten paragraph:

Figure 5 illustrates a typical hardware configuration of a computer system 500 which is representative of a hardware environment for practicing the present invention. Computer system 500 may have a central processing unit (CPU) 510 coupled to various other components by system bus 512. An operating system 540, may run on CPU 510 and provide control and coordinate the functions of the various components of Figure 5. An application 550 in accordance with the principles of the present invention may run in conjunction with operating system 540 and provide calls to operating system 540 where the calls implement the various functions or services to be performed by application 550. Application 550 may include, for example, a program for identifying pin locations to be used for diagonal interconnections as discussed in Figures 7A-D. Read only memory (ROM) 516 may be coupled to system bus 512 and include a basic input/output system ("BIOS") that controls certain basic functions of computer system 500. Random access memory (RAM) 514, I/O adapter 518 and communications adapter 534 may also be coupled to system bus 512. It should be noted that software components including operating system 540 and application 550 may be loaded into RAM 514 which may be the computer system's main memory. I/O adapter 518 may be a small computer system interface ("SCSI") adapter that communicates with a disk unit 520, e.g., disk drive. It is noted that the program of the present invention that identifies pin locations to be used for diagonal

interconnections, as discussed in Figures 7A-D, may reside in disk unit 520 or in application [[750]] 550.

(3) Please replace the paragraph beginning at line 16, page 16 with the following rewritten paragraph:

Figure 6 is a flowchart of one embodiment of the present invention of a method 600 for identifying pin locations in chip 110 (Figure 1) to be used for diagonal interconnections. Method 600 will be discussed in conjunction with Figures 7A-D depicting a spreadsheet 700 illustrating the calculated lengths of the orthogonal and diagonal interconnections as well as which particular pins are to be used for diagonal interconnections determined in accordance with the present inventive principles as explained in greater detail further below. It is noted that Figures 7A-D [[is]] are illustrative and is not to be construed in a limiting manner.

(4) Please replace the paragraph beginning at line 24, page 16 and ending at line 20, page 17 with the following rewritten paragraph:

Referring to Figure 6, in conjunction with Figures 4 and 7A-D, in step 601, the lengths of a plurality of orthogonal interconnections from a particular chip 110, e.g., chip 110A, to an adjacent chip 110, e.g., chip 110B, may be calculated. Referring to Figures 7A-D, a row 701 of orthogonal values, which may represent the length of orthogonal interconnections, thus calculated, where the values 702A-P represent distances in millimeters from pins in corresponding row/column combinations in adjacent chips 110. For example, the first value 702A in row 701 may refer to the distance between the pin position in chip 110, e.g., chip 110A, at row 451A/column 471 with the corresponding pin position in the adjacent chip 110, e.g., chip 110B. The first value may be a zero value because lengths in Figure 7 may be differential distances relative to the first length value. The second value 702B in row 701 may refer to the differential distance between the pin position in chip 110, e.g., chip 110A, at row 451B/column 471 with the corresponding pin in the adjacent chip 110, e.g., chip 110B, and so forth. The second value 702B, e.g., .8007 millimeters, may represent the additional distance in length to the first value length. It is noted that value 702P in row 701 represents the longest differential orthogonal distance,

e.g., 12.0102 millimeters, between the pin position in chip 110, e.g., chip 110A, at row 451P/column 171 and the corresponding pin in the adjacent chip 110, e.g., chip 110B. It is further noted that the orthogonal distances may be calculated using any column of adjacent chips 110 and that the above is illustrative. It is further noted that some of the values in row 701, e.g., value 702E, may refer to the differential distance between a pin position reserved for non-connecting purposes, e.g., power, ground, in chip 110, e.g., row 451E, column 471 in chip 110A, with the corresponding pin in the adjacent chip 110, e.g., chip 110B.

(5) Please replace the paragraph beginning at line 21, page 17 and ending at line 26, page 18 with the following rewritten paragraph:

In step 602, the lengths of a plurality of diagonal interconnections from a particular chip 110, e.g., chip 110A, to a diagonal chip 110, e.g., chip 110C, may be calculated. Referring to Figures 7A-B, spreadsheet 700 comprises rows 703A-N, where N may be any number, and columns labeled "A-P" used to indicate the lengths of calculated diagonal interconnections between diagonal chips 110. Rows 703A-N may collectively or individually be referred to as rows 703 or row 703, respectively. Each particular row/column combination may represent a particular pin location on a particular chip 110, e.g., chip 110A. Further, each particular row/column combination may comprise a value for a length of a particular diagonal interconnection. The value may represent the differential distance in millimeters with respect to the shortest orthogonal distance. That is, the value in each particular row/column combination in spreadsheet 700 may represent the length of a particular diagonal interconnection in millimeters that is additional to value 702A. (It is noted that the zero value for the differential distance in row 703A has been suppressed in Figures 7A-B because the corresponding pin located at row 451A/column 461A is reserved for non-connecting purposes.) For example, the value, e.g., .2003 millimeters, at row 703B/column "A" may refer to the additional distance in length to value 702A between the pin position in chip 110, e.g., chip 110A, at row 451B/column 461A with the corresponding pin in the diagonal chip 110, e.g., chip 110C. The value, e.g., .601 millimeters, at row 703C/column "A" may refer to the additional distance in length to value 702A between the pin position in chip 110, e.g.,

chip 110A, at row 451C/ column 461A with the corresponding pin in the diagonal chip 110, e.g., chip 110C. The value, e.g., 1.0017 millimeters, at row 703D/column "A" may refer to the additional distance in length to value 702A between the pin position reserved for non-connecting purposes, e.g., power, ground, in chip 110, e.g., chip 110A, at row 451D/ column 461A with the corresponding reserved pin position in the diagonal chip 110, e.g., chip 110C, and so forth. Hence, the values in rows 703 for each column may represent the value of the differential distance between the pin position in chip 110, e.g., chip 110A, at various rows 451 for a particular column 461 with the corresponding pin in the diagonal chip 110, e.g., chip 110C. The values in columns for each row 703 may represent the value of the differential distance between the pin position in chip 110, e.g., chip 110A, at various columns 461 for a particular row 451 with the corresponding pin in the diagonal chip 110, e.g., chip 110C, as described below.

(6) Please replace the paragraph beginning at line 3, page 20 and ending at line 14, page 20 with the following rewritten paragraph:

In step 604, a first number, e.g., sixteen, of available pin positions in a chip 110, e.g., chip 110A, associated with differential distances at or below the threshold value may be tagged with a first value, e.g., number "1", as illustrated in ~~the bottom portion of~~ Figure [[6]]7C. That is, a first number, e.g., sixteen, of pin positions not reserved for non-connecting purposes that are associated with differential distances at or below the threshold value may be tagged with a first value, e.g., number "1", as illustrated in ~~the bottom portion of~~ Figure [[6]]7C. The first number of pin positions tagged with the first value may be the pin positions in a chip 110, e.g., chip 110A, whose lengths for diagonal interconnections with corresponding pin positions in a diagonal chip 110, e.g., chip 110C, are at or below the threshold value. For example, referring to Figures 7A-D, each pin position tagged with the first value had a diagonal interconnection length smaller than 4.607 millimeters.

(7) Please replace the paragraph beginning at line 15, page 20 with the following rewritten paragraph:

In step 605, the remaining available pin positions may be tagged with a second value, e.g., number "0", as illustrated in ~~the bottom portion of~~ Figures [[6]]7C-D. That is, the remaining number of pin positions reserved for non-connecting purposes may be tagged with a second value, e.g., number "0", as illustrated in ~~the bottom portion of~~ Figures [[6]]7C-D. It is noted that not all of the pin positions that would be marked with the second value, e.g., number "0", are shown in Figures [[6]]7C-D for the purposes of readability.

(8) Please replace the paragraph beginning at line 21, page 20 and ending at line 5, page 21 with the following rewritten paragraph:

In step 606, a determination may be made as to whether the first number, e.g., sixteen, of pins tagged with a first value is an appropriate number of pin locations to be used for diagonal interconnections. That is, a determination may be made as to whether the first number of pins tagged with a first value is not too high or too low of a number of pin locations to be used for diagonal interconnections. If the first number, e.g., sixteen, of pins tagged is an appropriate number of pin locations to be used for diagonal interconnections, then, in step 607, the pin positions marked with a first value may be used for diagonal interconnections. The pattern formed by the set of pins used for diagonal interconnections may appear to form a triangular pattern as indicated by the triangular formed "1's" on ~~the bottom of~~ Figure [[6]]7C. Further, at least a portion of the pin positions marked with a second value may be used for orthogonal interconnections.